REMARKS

As a preliminary matter, on page 2 of the outstanding Office Action (second Paper No. 16), the Examiner has erroneously asserted that the changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 do not apply to the examination of this Application, because this Application was "not filed on or after November 29, 2000." In fact, the changes to Section 102(e) do apply to the present Application, because in the present Application, a Continued Prosecution Application was filed on March 4, 2002. Accordingly, all portions of the American Inventors Protection Act of 1999 apply to the present Application in their entirety, and the Examiner should withdraw his assertion to the contrary.

Claims 2-11 stand rejected under 35 U.S.C. 102(e) as being unpatentable over Ikeda et al. (US 5,815, 136). Applicant respectfully traverses this rejection because the cited reference does not disclose (or suggest) the memories of the present invention, which memories are recited to store information for controlling the display data of an image on a display unit, this information being different from the image data itself, as now recited in independent claims 2 and 8 of the present invention.

Ikeda discloses a liquid crystal display device which includes a liquid crystal panel 132, a CPU 1601, a main memory 1602, an address bus 1604, a data bus 1605, and a liquid crystal controller 1607. (See Fig. 16). The liquid crystal controller 1607 further includes an address converter 1608 and a timing control circuit 1610. Contrary to the Examiner's assertions, these elements of Ikeda are not the same as the asserted corresponding

features of the present invention, nor do they function the same as the recited features of the present invention.

For example, the Examiner asserts that the CPU 1601 "may include a lot of memories which is different from the main memory" 1602. This assertion is both unsupported and erroneous. The assertion is unsupported because Fig. 16 of Ikeda, and its corresponding description, neither teaches nor suggests in any way that the CPU 1601 may include "a lot of memories which is different from the main memory" 1602. The assertion is erroneous because Ikeda, in fact, teaches the opposite. Ikeda specifically teaches that an address in the CPU 1601 is directly transferred to the main memory 1602 through the address bus 1604. (See column 14, lines 12-14). In other words, Ikeda clearly teaches that the information in the CPU 1601 is the same as the information in the memory 1602. The memory 1602 receives through the address bus 1604 an address, *which is part of the image data*, that is output from the CPU 1601. Similarly, the memory 1602 directly transfers the remaining display data with the CPU 1601 through the data bus 1605. (See column 14, lines 59-62).

Ikeda even specifically diagrams in Figs. 17A and 17B the exact image data which is input and output from the CPU 1601. Ikeda further explains in column 14, lines 20-48 exactly how the data to and from the CPU 1601 is image information. In short, the only memories of Ikeda which were cited by the Examiner are specifically taught by Ikeda to only deal with image data. Applicant further notes that the Examiner, in his rejection, has not

actually even asserted that either the CPU 1601 or the main memory 1602 actually include memories which store information for controlling the display of data, as recited in claims 2 and 8. Accordingly, the Section 102 rejection is insufficient, and the cited reference otherwise fails to teach or suggest significant features of the present invention. For at least these reasons, the Section 102 rejection is respectfully traversed, and should be withdrawn.

Moreover, the Ikeda reference also fails to show other significant recited features of the present invention. Applicant submits that it is inappropriate for the Examiner to base his rejection solely on several of the recited elements of the present invention, while ignoring recited functions of such elements. Although some of the disclosed elements taught by Ikeda share similar labels with elements of the present invention, Ikeda neither teaches nor suggests that such elements also function as recited in the present invention. Ikeda's CPU 1601, data bus 1605, and address bus 1604 are not appropriately interpreted by the Examiner to constitute portions of the display device itself. These elements (and others) from Ikeda are more correctly considered to be part of a host or control-device, which is disclosed to be a separate device from the display device in the present invention. (See Fig. 3 of the present Application.)

For example, the Examiner asserts that the timing control circuit 1610 is analogous to the operation circuit of the present invention. The two circuits, however, are not analogous. The operation circuit of the present invention is recited to control the display unit to display image data based on information for controlling data display which is stored in

the recited memories. No such features are disclosed about the timing control circuit 1610 of Ikeda. The timing control circuit 1610 is only disclosed to receive a control signal from the control signal bus (Fig. 16; column 14, lines 50-52), and output a control signal to the control signal bus 103 or 1611. (See column 14, lines 52-58). Nowhere does Ikeda teach or suggest that any control signal is input from another bus, or that the signal from the control signal bus 1606 is based on information stored in the CPU 1601 or the main memory 1602.

More significantly, the present invention also specifically features that both the data bus and the address bus of the present invention connect the display control information memories of the present invention to the exterior of the display device to control the device. Ikeda, on the other hand, teaches just the opposite. Even if Applicant's arguments in the preceding paragraph were incorrect (which Applicant does not concede), and the timing control circuit 1610 of Ikeda could somehow control the display based on display information which "may be included" in one of the CPU 1601 or the main memory 1602, Ikeda still would teach the opposite of the present invention. Ikeda teaches that display control signals are provided to its control circuits only through the control signal bus 1606. In contrast, the present invention recites that such display control information connects through both the data bus and the address bus of the present invention. Ikeda does teach a data bus and an address bus, but only that display image data is transmitted through them. Accordingly, for these additional reasons, the section 102 rejection is further traversed.

Additionally, the present invention also recites that the address bus of the present invention supplies address signals for selecting one of the display control information memories. Ikeda teaches no such features. As discussed above, Ikeda teaches memories only for storing information related to image display. Additionally, all control information in Ikeda is transmitted only through the control signal bus 1606. Furthermore, one skilled in the art is apprised that control information memories, such as those of the present invention, are not typically accessed through an address bus to which a CPU is connected. The present invention is unique in this respect. Nowhere does Ikeda teach that display control information is transmitted through the address bus, or that display control information memories may be selected according to address signals supplied through the address bus. These features are clearly recited in the present invention, and distinct from any and all of the teachings of Ikeda. Accordingly, the Section 102 rejection should be withdrawn for these further reasons as well.

Applicant further respectfully traverses the rejection of claim 2 because the Examiner's remaining basis for the rejection is unsupported by the reference. The Examiner asserts that the driver 105-1 of Ikeda "controls by the timing control which is controlled by the CPU (memories) corresponding to the data driver." This assertion is unsupported because, as discussed above, nowhere does Ikeda teach that the CPU contains memories, or even that such memories could be anything other than image information. Furthermore,

nowhere does Ikeda even suggest that any potential memories in the CPU contain information to control the timing circuit.

Furthermore, the rejection of claim 2 is based on an erroneous assertion that information from the CPU 1601 is channeled to the driver 105-1 through the timing control circuit 1610. In fact, Ikeda actually teaches that an address is output from the CPU 1601into the address converter 1608 of the controller 1607, and through the address bus 1604. (See column 14, lines 12-18). Ikeda further teaches that the signal to the driver 105-1 actually comes directly from this address converter 1608 through the other address bus 101. (See column 14, lines 37-41). In other words, Ikeda again only teaches image information transmitted to the drivers from the CPU, without any suggestion in the reference of display control information from the CPU. The Examiner's assumptions as to what the reference "may" show, however, are an inappropriate basis for a Section 102 rejection. The Examiner should not guess at possibilities from a reference, but instead be required to show some objective support for his assumptions, or withdraw the rejection.

Similarly, with respect to claims 3-5, it is not enough for the Examiner to show only a shift register, a decoder, and an address counter in the cited reference. Such circuits are well known in the art. The Examiner instead is required to show support in the reference itself for how such circuits operate based on display control information stored in the recited memories of the present invention. In other words, it is inappropriate for the Examiner to reject these claims because they have some elements in common with the prior art. An

appropriate rejection must demonstrate all recited features of the claims, including the recited *relationship* between the several elements. These relationships are specifically recited in claims 3-5 of the present invention, and have been in no way established by the Examiner to be disclosed in the cited prior art reference. Accordingly, the rejection of claims 3-5 is further traversed.

With respect to claims 6-7 specifically, the Examiner has not even referred to the subject matter of these two claims of the present invention in his rejection of these claims based on the single cited prior art reference. Claim 6 of the present invention recites, among other things, that the display control information memories of the present invention store pattern data. The Examiner has also failed to assert in his rejection that Ikeda even teaches pattern data, or more particularly, pattern data for display control information, which is different from image data. Accordingly, the rejection of claim 6 must also be withdrawn.

The rejection of claim 7 is even further lacking. First, claim 7 depends on claim 6, and the rejection must be withdrawn for at least the reasons discussed above with respect to claim 6. Second, the rejection must be withdrawn because the Examiner has not even asserted that Ikeda teaches anything like the data-synthesis circuit recited in claim 7 of the present invention. Claim 7 recites that the data-synthesis circuit of the present invention functions to combine the pattern data, stored in the display control information memories of the present invention, with the display data itself. Not only does Ikeda entirely fail to teach or suggest any such features, but these features from claim 7 even more particularly illustrate

the differences between the recited display control information and image information. After five separate Amendments and Responses, all of which specifically highlighted these differences between these two types of information, the Examiner has not once disputed any of the many meritorious arguments explaining the distinction. Accordingly, with these even further reasons, the outstanding Section 102 rejection must be withdrawn with respect to claim 7, as well as the invention as a whole.

With respect to claim 8 of the present invention specifically, Applicant notes that the Examiner has based his rejection of claim 8, not on any teaching from the specification of Ikeda, but instead on a single clause from one of Ikeda's several claims. In fact, the claimed text cited by the Examiner in column 42, lines 59-64, claims nothing more than the address converter 1608, which is already discussed above with respect to Fig. 16 of Ikeda. If anything, this cited claim text actually supports Applicant's many previous arguments by teaching that only image information is included in the display memory. In fact, the Examiner here even contradicts his own rejection by asserting that the display information memories recited in claim 8 of the present invention are equivalent to the display memory recited in claim 14 of Ikeda. The display memory recited in claim 14 is actually the very same memory the Examiner has elsewhere asserted to be equivalent to the display control information memories of the present invention. Once again, Applicant requests that the Examiner acknowledge the distinction clearly recited between the two different kinds of memories in the present invention, and withdraw the rejection.

With respect to the Examiner's rejection of claim 9, Applicant respectfully traverses because rejection does not address the actual recited features of the claim itself. claim 9 specifically recites, among other things, that the display information acquisition circuit (recited in claim 8) of the present invention checks the display unit to acquire information with regard to a defect of the display unit. The portion of text from Ikeda cited by the Examiner, however, discloses no information of how an acquisition circuit may obtain information regarding a defect of the display unit. Ikeda's latch circuit 187, 189, as noted by the Examiner, only allows display operation at a fixed period in the case where updating access and display access of Ikeda's device overlap. Such overlapping access has nothing to do with a defect in the display unit itself, or how an acquisition circuit obtains such defect data. Accordingly, because the Examiner has cited no information from Ikeda regarding the subject matter of claim 9, the rejection of this claim must be withdrawn as well.

With respect to claim 10 of the present invention, Applicant respectfully traverses the rejection because the Examiner has similarly cited nothing from Ikeda which teaches how an acquisition circuit may obtain information about the display unit with respect to coordinates of a position at which input is entered on the display unit. As the basis for the rejection of this claim, the Examiner has again cited only that text portion from claim 14 of Ikeda regarding the address converter previously discussed. Ikeda's address converter, however, is only disclosed by Ikeda to provide address information to the display unit, but nowhere does Ikeda teach or suggest that its address converter can acquire information about

the display unit itself. More particularly, nothing about Ikeda's address converter is disclosed to be able to acquire information from the display unit with regard to coordinates of a position at which input is entered on the display unit. Ikeda merely discloses that the address converter can provide display information regarding the position where display information may be entered, but nowhere does Ikeda teach that this address converter may also acquire information about the coordinates of the input data on the display unit after the data is input on the unit. Accordingly, for at least these reasons as well, the rejection of claim 10 of the present invention is respectfully traversed, and should be withdrawn.

For all of the foregoing reasons, Applicant submits that this Application, including claims 2-11, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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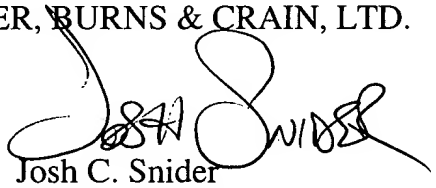
By 

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